

IN THE CLAIMS:

- 1 1. (Previously presented) A serializer arranged to accept a data word from a computing
2 system and to send the data word out bit by bit, the serializer comprising:
3 means for serially outputting the data word via a data line of an output port, the
4 means for serially outputting having a control input; and
5 a first bit clock connected to the control input wherein the data bits are serially
6 sent out, and wherein the first bit clock is synchronized to the define the individual bits
7 being sent out, and wherein the first bit clock is sent out via bit clock lines of the output
8 port, the bit clock in parallel with the data bits.
- 1 2. (Original) The serializer of claim 1 further comprising means for obtaining the data
2 word from a bi-directional data bus of the computing system.
- 1 3. (Original) The serializer of claim 1 further comprising means for sending a word
2 boundary comprised of a combination of signals on the bit clock and the data lines of the
3 serial port.
- 1 4. (Withdrawn) A deserializer arranged to receive a data word bit by bit and present the
2 data word to a computing system, the deserializer comprising:
3 means for serially receiving the data word bits from a data line of a serial input
4 port, the means for serially receiving data having a control input; and
5 a bit clock signal synchronized to define the individual bits being received, the bit
6 clock received from a bit clock line of the serial input port, and wherein the bit clock is
7 connected to the control input wherein the data word bits are serially received.
- 1 5. (Withdrawn) The deserializer of claim 4 further comprising means for sending the
2 received data word to the computing system is via a bi-directional data bus.

1 | 6. (Withdrawn) The deserializer of ~~claim 3~~claim 4 further comprising means for receiv-
2 ing and detecting a word boundary comprised of a combination of signals on the received
3 bit clock line and the data line.

1 7. (Previously presented) A serializer/deserializer, the serializer portion arranged to ac-
2 cept a first data word from a computing system and to send the first data word out bit by
3 bit, and the deserializer portion arranged to receive a second data word bit by bit and pre-
4 sent the second data word to the computing system, the serializer/deserializer comprising:
5 means for serially outputting the first data word via a data line of a serial port;
6 the means for serially outputting having a control input;
7 a first bit clock connected to the control input wherein the first data bits are seri-
8 ally sent out, and wherein the first bit clock is synchronized to define the individual bits
9 being sent out, and wherein the first bit clock is sent out via a bit clock line of the serial
10 port, the first bit clock in parallel with the data bits;
11 means for serially receiving second data word bits from the data line of the serial
12 port, the means for serially receiving having a second control input; and
13 a second bit clock signal synchronized to define the individual bits being re-
14 ceived, the second bit clock received from the bit clock line of the serial port, and
15 wherein the second bit clock is connected to the second control input wherein the second
16 data word bits are serially received.

1 8. (Previously presented) The serialzer/deserializer of claim 7 further comprising means
2 for obtaining the first data word from a bi-directional data bus of the computing system,
3 and means for sending the received second data word to the computing system is via the
4 bi-directional data bus.

1 9. (Previously presented) The serializer/deserializer of claim 7 further comprising means
2 for forming and sending a first word boundary comprised of a combination of signals on
3 the bit clock line and the data line of the serial port, and means for receiving and detect-

4 ing a second word boundary comprised of a combination of signals on the bit clock line
5 and the data line of the serial port.

1 10. (Previously presented) The serializer/deserializer of claim 7 further comprising
2 means for controlling the sending and the receiving of data and bit clock over the serial
3 data port.

1 11. (Previously presented) A process for serializing that is arranged to accept a data
2 word from a computing system and to send the data word out bit by bit, the process com-
3 prising the steps of:
4 serially outputting the data word via a data line of an output port;
5 controlling the serial outputting with a control input;
6 connecting a first bit clock to the control input wherein the data bits are serially
7 sent out, and wherein the first bit clock is synchronized to define the individual bits being
8 sent out; and
9 sending the first bit clock out via bit clock lines of the output port, the bit clock in
10 parallel with the data bits.

1 12. (Previously presented) The process of serializing of claim 11 further comprising the
2 step of:
3 obtaining the data word from a bi-directional data bus of the computing system.

1 13. (Original) The process of serializing of claim 11 further comprising the step of:
2 sending a word boundary comprised of a combination of signals on the bit clock
3 and the data lines of the serial port.

1 14. (Withdrawn) A process of de-serializing that is arranged to receive a data word bit
2 by bit and present the data word to a computing system, the process comprising the steps
3 of:
4 serially receiving the data word bits from a data line of a serial input port;

5 controlling the serially receiving data with a control input;
6 receiving a bit clock from a bit clock line of the serial input port, the bit clock
7 synchronized to define the individual bits being received; and
8 connecting the bit clock to the control input wherein the data word bits are serially
9 received.

1 15. (Withdrawn) The process of de-serializing of claim 14 further comprising the step
2 of:

3 sending the received data word to the computing system via a bi-directional data
4 bus.

1 16. (Withdrawn) The process of de-serializing of claim 14 further comprising the step
2 of:

3 receiving and detecting a word boundary comprised of a combination of signals
4 on the received bit clock line and the data line.

1 17. (Previously presented) A process for serializing and de-serializing, the serializing
2 portion arranged for accepting a first data word from a computing system and sending the
3 first data word out bit by bit, and the de-serializing portion arranged for receiving a sec-
4 ond data word bit by bit and presenting the second data word to the computing system,
5 the process for serializing and de-serializing comprising the step of:

6 serially outputting the first data word via a data line of a serial port, the means for
7 serially outputting having a control input;

8 connecting a first bit clock to the control input wherein the first data bits are seri-
9 ally sent out, and wherein the first bit clock is synchronized to define the individual bits
10 being sent out;

11 sending out the first bit clock via a bit clock line of the serial port, the first bit
12 clock in parallel with the data bits;

13 serially receiving second data word bits from the data line of the serial port, the
14 means for serially receiving data having a second control input; and

15 receiving a second bit clock signal from the bit clock line of the serial port, the
16 second bit clock synchronized to define the individual bits being received, and wherein
17 the second bit clock is connected to the second control input wherein the second data
18 word bits are serially received.

1 18. (Previously presented) The serializing and de-serializing of claim 17 further com-
2 prising the steps of:

3 obtaining the first data word from a bi-directional data bus of the computing sys-
4 tem, and sending the received second data word to the computing system is via the bi-
5 directional data bus.

1 19. (Previously presented) The serializing and de-serializing of claim 17 further com-
2 prising the steps of: forming and sending a first word boundary comprised of a combina-
3 tion of signals on the bit clock line and the data line of the serial port; and

4 receiving and detecting a second word boundary comprised of a combination of
5 signals on the bit clock line and the data line of the serial port.

1 20. (Previously presented) The serializing and de-serializing of claim 17 further com-
2 prising the step of:

3 controlling the sending and the receiving of data and bit clock over the serial data
4 port.